

CLAIMS

1. In a communication system, a buffer management system for managing communication packets received from multiple I/O ports, said system comprising:

5 on-chip memory for storing at least a free data pointer and a buffer descriptor;

the free data pointer pointing to a data buffer allocated in external memory;

10 the buffer descriptor including at least a data pointer pointing to a data buffer configured to store one or a portion of the communication packet;

15 the on-chip memory having a maximum threshold such that if the number of buffer descriptors stored in the on-chip memory reaches the maximum threshold one or more buffer descriptors stored in on-chip memory are transferred to an external memory.

2. The buffer management system of claim 1, wherein:

when one or a portion of a communication packet is received, a free data pointer is removed from the on-chip memory; said one or a portion of the communication packet is stored in a data buffer pointed to by the free data pointer; a buffer descriptor is generated including the free data pointer; and the buffer descriptor is stored in the on-chip memory.

3. The buffer management system of claim 2, wherein:

one or more free data pointers are stored in external memory; and

25 the on-chip memory has a minimum threshold for the number of free data pointers stored in the on-chip memory such that if the minimum threshold is met one or more free data pointers are transferred from external memory to on-chip memory.

4. The buffer management system of claim 2, further comprising a direct memory access controller for transferring buffer descriptors and data pointers between on-chip memory and the external memory.

5 5. The buffer management system of claim 2, wherein the on-chip memory includes a read free queue wherein said one or more free data pointers are stored.

10 6. The buffer management system of claim 5, wherein the on-chip memory further includes a receive ready queue wherein one or more buffer descriptors are stored.

15 7. The buffer management system of claim 6, wherein the on-chip memory further includes a transmit ready queue associated with an I/O port, wherein one or more buffer descriptors generated for a communication packet destined for the I/O port are transferred from the receive ready queue to the transmit ready queue for the I/O port.

20 8. The buffer management system of claim 7, wherein the on-chip memory further includes a write free queue for storage of a freed data pointer after the communication packet associated with that data pointer is transmitted.

25 9. The buffer management system of claim 7, including a plurality of transmit ready queues associated with a plurality of I/O ports, wherein transmission priority of communication packets is programmable based on the priority assigned to de-queuing buffer descriptors stored in the transmit ready queues.

30 10. The buffer management system of claim 2, wherein the on-chip memory comprises a receive ready queue for storing one or more buffer descriptors, said receive ready queue including a write FIFO and a read FIFO; wherein:

newly generated buffer descriptors for received communication packets are written to the write FIFO;

buffer descriptors written to the write FIFO are moved to the read FIFO, if the read FIFO is below a maximum threshold level; otherwise

5 buffer descriptors written to the write FIFO are transferred to external memory;

 buffer descriptors transferred to external memory are moved to the read FIFO if the read FIFO is below a maximum threshold level.

10 11. A method for receiving communication packets in a communication system using a buffer management system, said method comprising:

 removing a data pointer from an on-chip read free queue, the read free queue having a minimum threshold, the data pointer pointing to a data buffer allocated in external memory for storing one or a portion of a communication packet;

15 storing in the data buffer one or a portion of a communication packet received by an I/O port;

 generating a buffer descriptor including at least the data pointer;

 storing the buffer descriptor in an on-chip receive ready queue;

20 wherein the receive ready queue has a maximum threshold such that if the maximum threshold is reached one or more buffer descriptors stored in the receive ready queue are transferred to external memory.

12. The method of claim 11 wherein the buffer descriptor is generated if

25 end of a communication packet is detected.

13. The method of claim 11 wherein the buffer descriptor is generated if the data buffer is full.

30 14. The method of claim 11 further comprising:

if the receive ready queue is not empty then a processor reading a buffer descriptor from the receive ready queue.

15. The method of claim 12 further comprising:

5 if the receive ready queue reaches a minimum threshold then transferring one or more buffer descriptors, if any, from the external memory to the receive ready queue.

16. The method of claim 14 further comprising:

10 the processor processing one or more descriptor fields in the buffer descriptor.

17. The method of claim 16 wherein one of said one or more descriptor fields is a length field indicating the length of data stored in the data buffer
15 associated with the buffer descriptor.

18. The method of claim 16 wherein one of said one or more descriptor fields is a status field indicating whether the data stored in the data buffer associated with the buffer descriptor is error free.

20 19. The method of claim 16 wherein one of said one or more descriptor fields is a type field indicating whether the buffer descriptor is associated with a data buffer storing the beginning, middle, or end of a communication packet.

25 20. The method of claim 16 wherein one of said one or more descriptor fields is a destination field indicating the destination of one or portion of a communication packet stored in the data buffer associated with the buffer descriptor.

21. The method of claim 16 further comprising:

30 the processor determining the destination of transmission of the communication packet associated with the buffer descriptor.

22. The method of claim 21 further comprising:

if the communication packet is to be transmitted to another I/O port other than the I/O port it was received then copying the buffer descriptor to an on-chip transfer ready queue associated with the destination I/O port.

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23. The method of claim 21 further comprising:

if the communication packet is to be transmitted to another I/O port other than the I/O port it was received then returning the data pointer associated with the buffer descriptor to an on-chip write free queue having a maximum threshold.

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24. The method of claim 23 further comprising:

if the write free queue has reached its maximum threshold then transferring free data pointers to external memory.

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25. The method of claim 24 further comprising:

if the read free queue has reached its minimum threshold then transferring free data pointers in the external memory, if any, to the read free queue.

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26. The method of claim 25 further comprising:

the destination I/O port reading a BD from the transfer ready queue if the transfer ready queue is not empty.

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27. The method of claim 26 further comprising:

the destination I/O port transmitting the communication packet associated with the BD to a destination node based on destination information stored in the BD.

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28. The method of claim 11 wherein the receive ready queue includes a write FIFO and a read FIFO, the storing step comprising:

writing the generated buffer descriptor to the write FIFO;

if the read FIFO is below a maximum threshold level then moving the buffer descriptor in the write FIFO to the read FIFO.

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29. The method of claim 28 further comprising:

if the read FIFO's level is above a maximum threshold then transferring the buffer descriptor in the write FIFO to the external memory.

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30. The method of claim 29 further comprising:

moving the buffer descriptors in the external memory to the read FIFO if the read FIFO falls below the maximum threshold.

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31. A method for managing communication packets using a buffer management system, said method comprising:

removing a data pointer from an on-chip read free queue, the read free queue having a minimum threshold, the data pointer pointing to a data buffer allocated in external memory for storing one or a portion of a communication packet;

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storing in the data buffer one or a portion of a communication packet constructed by a software application;

generating a buffer descriptor including at least the data pointer;

storing the buffer descriptor in an on-chip receive ready queue;

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wherein the receive ready queue has a maximum threshold such that if the maximum threshold is reached one or more buffer descriptors stored in the receive ready queue are transferred to external memory.

32. The method of claim 31 wherein the buffer descriptor is generated if

30 end of a communication packet is detected.

33. The method of claim 31 wherein the buffer descriptor is generated if the data buffer is full.

34. The method of claim 31 further comprising:

5 if the receive ready queue is not empty then a processor reading a buffer descriptor from the receive ready queue.

35. The method of claim 32 further comprising:

10 if the receive ready queue reaches a minimum threshold then transferring one or more buffer descriptors, if any, from the external memory to the receive ready queue.

36. The method of claim 34 further comprising:

15 the processor processing one or more descriptor fields in the buffer descriptor.

37. The method of claim 36 wherein one of said one or more descriptor fields is a destination field indicating a destination address for one or portion of a communication packet stored in the data buffer associated with the buffer descriptor.

20 38. The method of claim 37 further comprising:

transferring the buffer descriptor to an on-chip transmit ready queue for an I/O port associated with the destination address.

25 39. The method of claim 38 further comprising:

I/O port reading the buffer descriptor from on-chip transmit ready queue.

40. The method of claim 39 further comprising:

30 I/O port returning the data pointer associated with the buffer descriptor to an on-chip write free queue.

41. A method for managing interleaved communication streams in a communication system comprising:

generating a buffer descriptor having type and status data; said buffer descriptors associated with one or a portion of a communication packet stored in a data buffer allocated in an external memory; the type data indicating whether the buffer descriptor is associated with a data buffer that stores beginning, middle, or end of a communication packet; the status data indicating the communication channel from which the communication packet was received;

10 storing the buffer descriptor in on-chip memory;

 reading the buffer descriptor from on-chip memory;

 moving the buffer descriptor from on-chip memory to a buffer in external memory associated with the communication channel identified by the status data;

15 examining the type data for the buffer descriptor; and

 if the type data indicates that the buffer descriptor is associated with a data buffer that stores the end of a communication packet then notifying a higher layer application that a communication packet is received.

20 42. In a communication system, a buffer management system for

managing communication packets received from multiple I/O ports, said system comprising:

 a first memory for storing at least a free data pointer and a buffer descriptor;

25 the free data pointer pointing to a data buffer allocated in a second memory;

 the buffer descriptor including at least a data pointer pointing to a data buffer configured to store one or a portion of the communication packet;

 the first memory having a maximum threshold such that if the 30 number of buffer descriptors stored in the first memory reaches the

maximum threshold one or more buffer descriptors stored in the first memory are transferred to the second memory.

43. The system of claim 42, wherein the first memory is accessible faster
5 than the second memory.

43. The system of claim 42 further comprising:
the first memory having a minimum threshold such that if the number
of buffer descriptors stored in the first memory reaches the minimum
10 threshold one or more buffer descriptors stored in the second memory are
transferred to the first memory.